REMARKS

Present Status of the Application

Claims 1-9 are still pending of which the claims 1-5 and 7-9 have been amended without prejudice or disclaimer in order to more explicitly describe the claimed invention. However, applicant respectfully traverses the preceding rejection based on the following arguments. For at least the foregoing reasons, applicants respectfully submit that claims 1-9 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion for amendments to specification

The paragraph [0012] is so amended to indicate TTL stands for transistor-transistor logic, which is known in the art. Thus, amendment to paragraph [0012] does not introduce any new matter.

Discussion for title of the invention:

2. The bracket in the title needs to be removed.

This application is electronically filed, wherein the brackets in the title are inserted automatically by the ESF system. Withdrawal of the objection is thereby respectfully requested.

Discussion for objection to claims 1, 3-4

3. Claims 1, 3-4 are objected due to their informalities.

In response thereto, claims 1, 3-4 are amended as instructed by the Examiner.

Discussion for objection to claims under 35 U. S. C. 112, 1st paragraph

6-8. Claims 2-4, 5, 8-9 are rejected because Examiner cannot find their limitation have been supported.

In re claim 2, the limitation, "a control signal latch coupled to the bus interface unit via the internal data bus, wherein the data output latch is a latch for latching a control signal transmitted by the nonreal-time data interface unit to other units," is amended to "a control signal latch coupled to the bus interface unit via the internal data bus, wherein the data output latch is a latch for latching a control signal transmitted **from** the nonreal-time data interface unit to other units." This amendment is supported in paragraph [0027], part of which is recited as follows:

[0027] In addition, the internal control signal of the nonreal-time data interface unit 210 and the control signal of other functional block of the present invention are cached in a control signal latch 307 via the internal data bus 31. Then, the control signal for controlling other functional block of the present invention is propagated via a control bus.

Likewise, claims 5, 8-9 are so amended to more clarify limitations as alleged by the Examiner. For example, in claim 8, the limitation, "the TTL/differential level converting interface is used to convert ..., and to cache the real-time data" is amended to cancel the phrase, "and to cache the real-time data" because this phrase is not supported in specification.

Discussion for objection to claims under 35 U. S. C. 112, 2nd paragraph

9. Claims 2-5, 7-9 are rejected under 35 U. S. C. 112, 2nd paragraph as being indefinitely for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In response thereto, claims 2-5, 7-9 are so amended to particularly point out and distinctly claim the subject matter which applicant regards as the invention. However, applicant respectfully clarifies that "internal data bus" (i.e. reference numeral 31 in

Fig.2) **recited in claim 2** is used to transfer both data and control signal so that an internal control bus as suggested by Examiner is not needed.

Discussion for rejection to claims under 35 U. S. C. 102(b)

5. Claims 1 is rejected under 35 U .S. C. 102(b) as being anticipated by Kuver et al. (US 6, 438,604)

In response thereto, applicants respectfully traverses the preceding rejection based on the following arguments. First of all, to establish a prima facie case of anticipation, the cited reference (i.e. Kuver) should teach all limitations of the claim 1.

The amended claim 1 is partly recited as follows:

A real-time data transmission interface **coupled between a radar system for providing real-time data and a host computer for providing nonreal-time data, suitable for transmitting the nonreal-time data in real-time from the host computer to the radar system and transmitting the real-time data in nonreal-time from the radar system to the host computer.**(emphasis added)

From Fig.2 and abstract in Kuver, network interface (4) alleged as claimed real-time data transmission interface by the Examiner, is not coupled between a host computer and radar system as claimed in amended claim 1. **Claim 1 differs Kuver in that Kuver discloses a one-way data transmission from a transmitting DV camera to a receiving DV camera but the claim1 claims bi-directional data transmission between a host computer and a radar system.** Furthermore, the Examiner alleged that claimed limitation "transmitting nonreal-time data in real-time" is disclosed in recitation "data from asynchronous network being transmitted isochronously to a camera" in abstract in Kuver. However, applicant respectfully disagrees the Examiner's allegation because the word "isochronously" cannot be

interpreted as "real-time" at all. In fact, the phrase "transmitted isochronously" means that each data takes the same time for transmitting data from transmitting terminal to receiving terminal. Whereas, claimed phrase "transmitting in real-time" means that time for transmitting data from transmitting terminal to receiving terminal, is almost zero. Thus, Kuver fails to teach, suggest or disclose "A real-time data transmission interface coupled between a radar system for providing real-time data and a host computer for providing nonreal-time data, **suitable for transmitting the nonreal-time data in real-time from the host computer to the radar system and transmitting the real-time data in nonreal-time from the radar system to the host computer,**" as claimed in amended claim 1. That is, the amended claim 1 is not anticipated by Kuver and thus patentable.

Discussion for rejection to claims under 35 U. S. C. 103(a)

15. Claims 2-7are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuver

In response thereto, applicant respectfully traverses the rejection based on the following arguments. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine references teachings. Second, there must be a reasonable expectation of success. **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The Examiner cannot establish a prima facie case of obviousness by only alleging that elements as claimed in claims 2-7 are known in the art. Thus, Kuver cannot render claims 2-7 obvious because a prima facie case of obviousness is not well established. That is, claims 2-7 are patentable.

21. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuver in view of Christopher (US 5,220,211) AND Kosaraju (US6, 907, 490).

In response thereto, likewise, by using the preceding argument, combination of Kuver and Christopher cannot render claim 8 obvious because the claimed TTL/differential level converting interface is not identical to CV1, CV2 (signal converter circuit) shown in Fig.2 in Christopher. Thus, claim 8 is patentable. Moreover, claim 9 is patentable based on the same arguments as applied to claims 2-7.

Additionally, since claims 2-9 are dependent claims, they should be patentable as a matter of law for the reason they contain all limitations of their base amended claim 1.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-9 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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